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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,127	08/18/2003	YuQing Yang	1339-CA (P192 C1)	3503

7590 08/20/2004

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EXAMINER	
JEAN PIERRE, PEGUY	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,127	YANG ET AL.	
	Examiner	Art Unit	
	Peguy JeanPierre	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16,17 and 28-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,17 and 28-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 16-17 and 28-37 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 16 and 28, lines 10, the term "the integration capacitor...(added limitation)" lacks antecedent basis. The term has not been previously recited.

In addition, lines 11-12, the term "...common node to an integration capacitor..." is unclear. It seems to refer to the integration capacitor previously recited.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 16-17 and 28-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujimori (USP 5,790,064).

Fujimori discloses in Figure 3 a method of operating a switched capacitor integrator that operates to sample (ϕ1D) a reference voltage of a selected polarity (Vref) into an input plate (Crp) or (another capacitor) of a reference capacitor, sample (ϕ1D) an input signal onto a sampling (Cs) capacitor or (a capacitor), both sampling phases occur

on the same sampling phase (ϕ1D) (see col. 2, lines 55-60). During a first period of an integrating phase (ϕ2D) transfer the sampled charges from the reference and input sampling capacitors to a common node by closing on switches (ϕ21D) and (ϕ1) and during a second phase of the integration phase transferring all of the charges from the common node (node coupled to (Cs or Crp) and (ϕ2)) to an integrating capacitor (Ci). Figure 6 further discloses the graph of the sampling (ϕ1 and ϕ1D) integrating (ϕ2 and ϕ2D) phases of the switching circuitry that can be accurately implemented in response to a control signal (see Fig. 7). In Figure 8, Fujimori also discloses a delta sigma modulator that forms a portion of an analog to digital converter. The modulator comprises an integrator (50), an operational amplifier 52) and a DA converter (54). The integrator as illustrated in Figure 3, further comprises an operational amplifier that comprises an integration capacitor (Ci) that couples an output of the operational amplifier to an input node of the amplifier, a first and a second feedback paths each including a capacitor that sample reference charges (Vref, Vref-) of selected polarities onto the first and the second capacitors during the sampling phase. In addition, Fujimori discloses another capacitor (that can be considered as a third capacitor) that samples the input signal source during a sampling phase (see Fig. 3).

Response to Arguments

4. Applicant's arguments filed on 7/2/2004 have been fully considered but they are not persuasive. Applicant argues that in the present invention during the integration phase charge is transferred from the input and reference capacitors to the common nodes and then the common nodes are coupled to the integration capacitors whereas in

the cited reference (Fujimori) the order of operation is reverse. The Examiner disagrees. The Examiner maintains that both the present invention and the cited reference have two phases of operation, a sampling phase and an integration phase and both circuits operate the same way. (ϕ1) which represents the sampling phase when the input and the reference voltages are sampled onto a sampling capacitor and (ϕ2) the integration phase when the charges are transferred from the nodes to the integrating capacitors. Both the reference and the present invention have their nodes coupled to the input of an amplifier and a switch that is "on" during the integration phase coupled between the nodes and integrating capacitors.

Applicant also argues that only after the sampling capacitors (Cs, Crn, Crp) are all coupled to the amplifier summing nodes, are the sampled charges transferred during integration sub-phase (ϕ2d), it appears that the present invention operates the same way.

It is also to be noted that that has two integration periods. For instance in a first integration period (ϕ2d) input and reference signals are transferred to a common node and during a second period of integration phase (ϕ2) the common node and the integrating capacitors are coupled to transfer sampled charges from the common node to the integrating capacitors. Hence, in response to Applicant's argument the Examiner notes that all the charges are not dumped at once to the amplifier input summing node for there are two integration periods.

Applicant argument/remark does not provide a clear distinction between the cited art and the present invention.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peguy JeanPierre whose telephone number is (571) 272-1803272-1803. The examiner fax phone number is (571) 273-1803.

Peguy JeanPierre
Primary Examiner